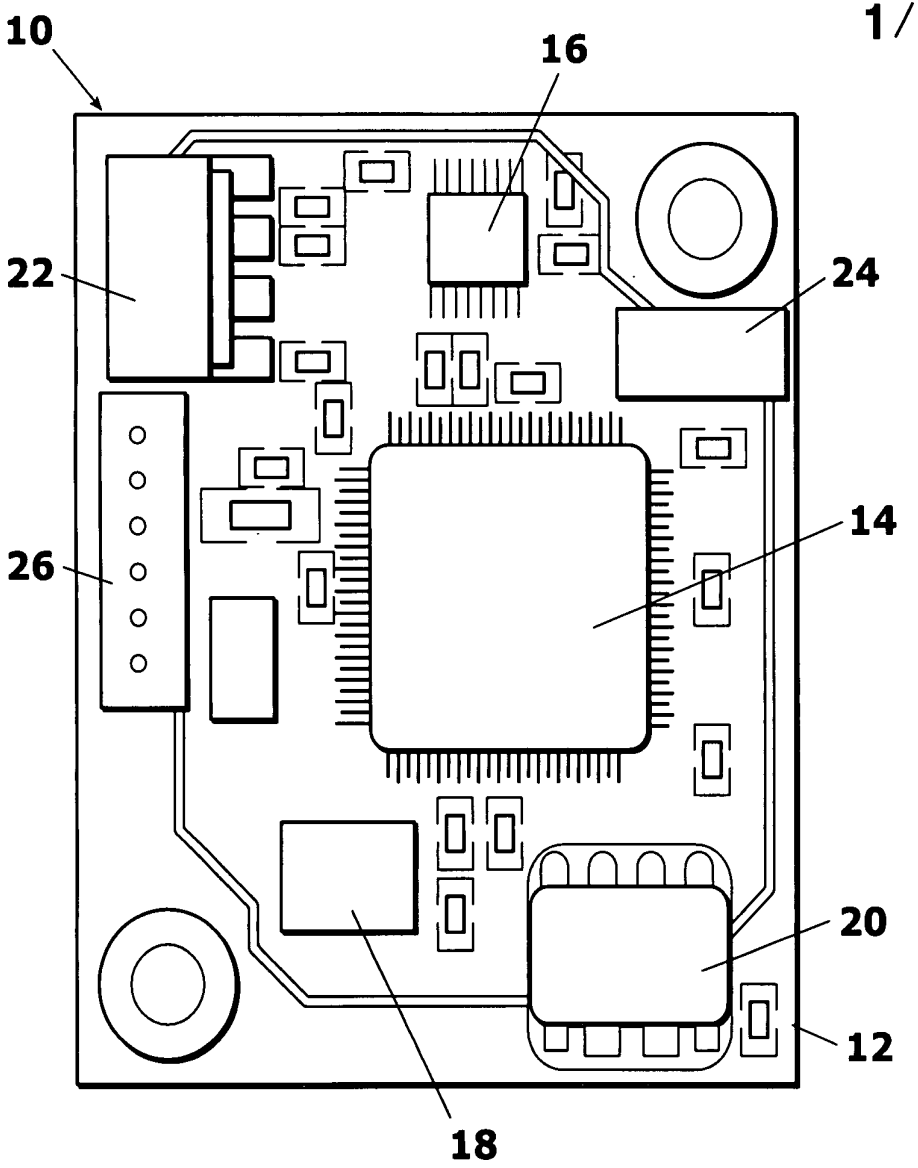


Fig. 1

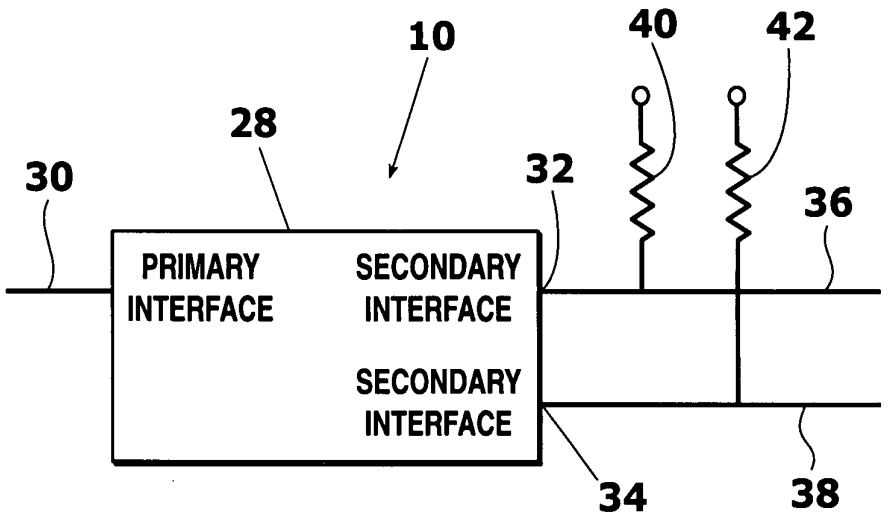


Fig. 2

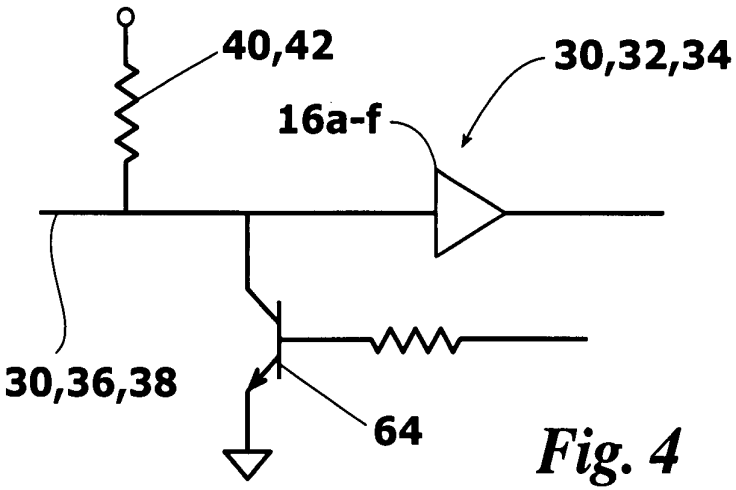


Fig. 4

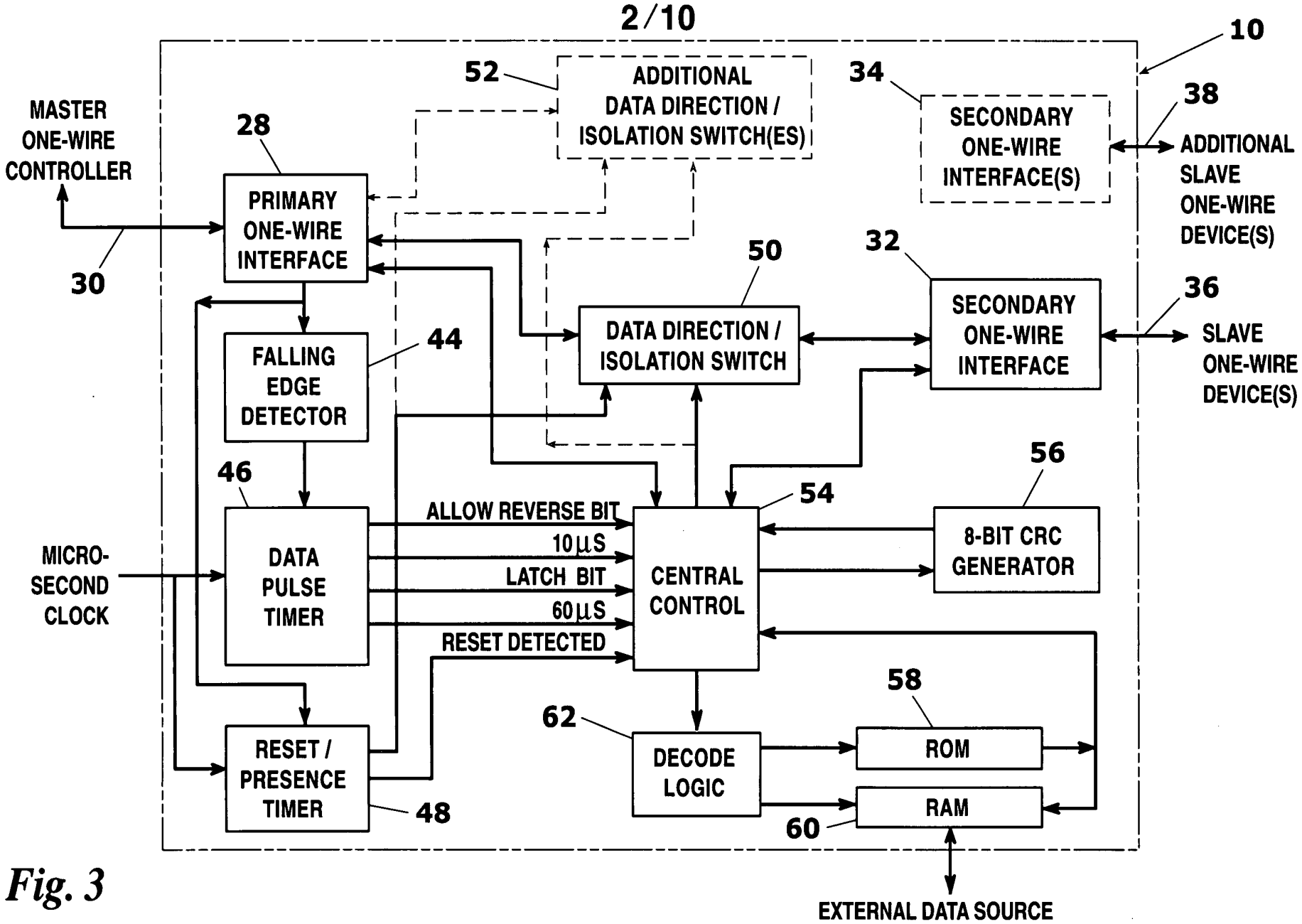

10
52
ADDITIONAL DATA DIRECTION / ISOLATION SWITCH(ES)
34
SECONDARY ONE-WIRE INTERFACE(S)
38
ADDITIONAL SLAVE ONE-WIRE DEVICE(S)
MASTER ONE-WIRE CONTROLLER
28
PRIMARY ONE-WIRE INTERFACE
30
50
32
DATA DIRECTION / ISOLATION SWITCH
SECONDARY ONE-WIRE INTERFACE
36
SLAVE ONE-WIRE DEVICE(S)
FALLING EDGE DETECTOR
44
46
56
54
ALLOW REVERSE BIT
10µS
LATCH BIT
60µS
RESET DETECTED
MICRO-SECOND CLOCK
DATA PULSE TIMER
CENTRAL CONTROL
8-BIT CRC GENERATOR
58
62
RESET / PRESENCE TIMER
48
DECODE LOGIC
ROM
RAM
60
EXTERNAL DATA SOURCE

Fig. 3

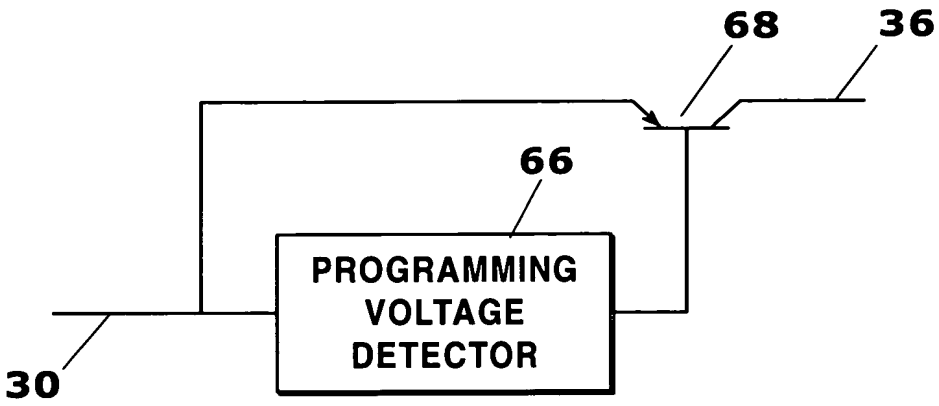

68
36
66
PROGRAMMING VOLTAGE DETECTOR
30

Fig. 5

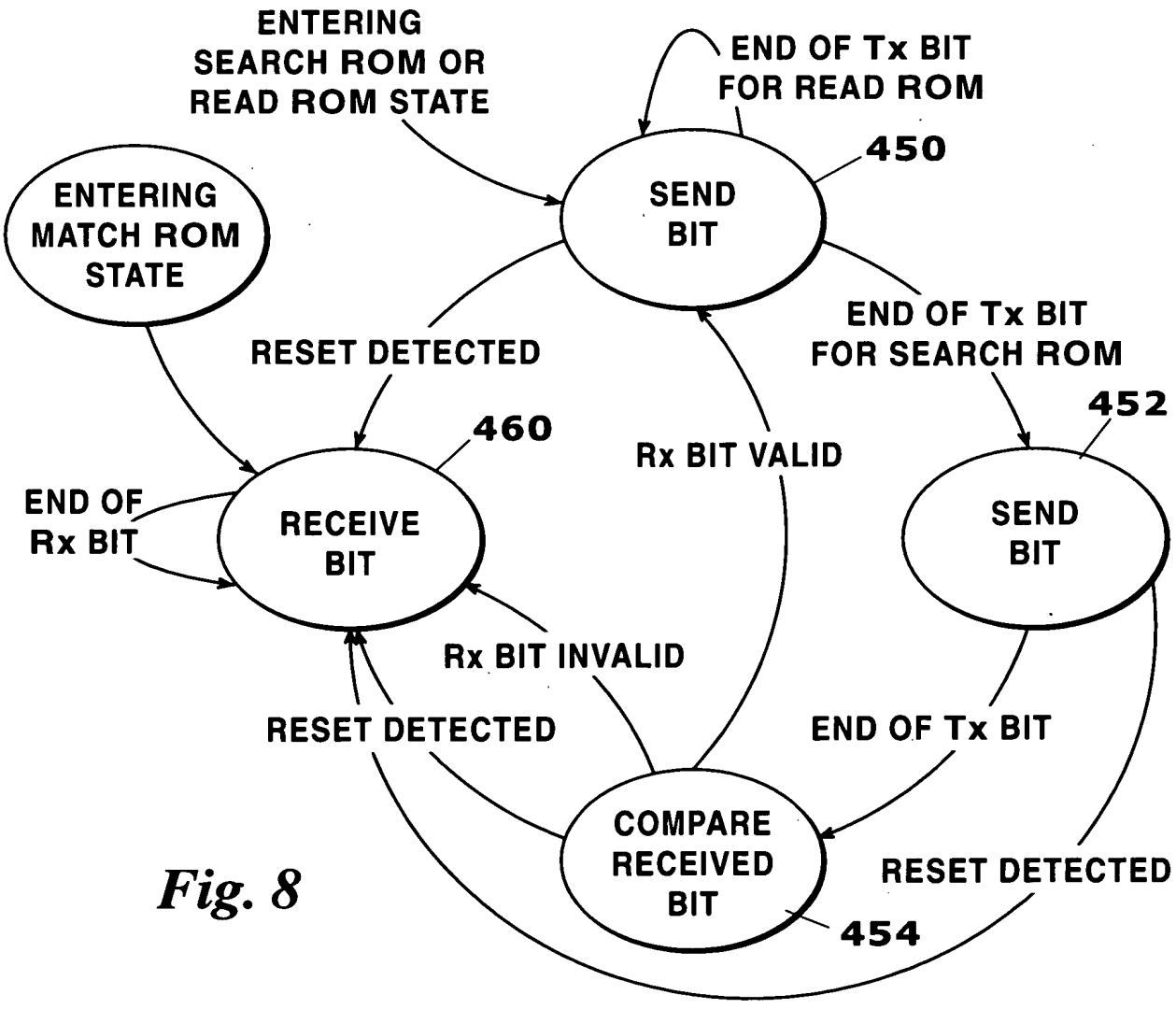

ENTERING SEARCH ROM OR READ ROM STATE
END OF Tx BIT FOR READ ROM
450
SEND BIT
ENTERING MATCH ROM STATE
RESET DETECTED
END OF Tx BIT FOR SEARCH ROM
452
460
Rx BIT VALID
END OF Rx BIT
RECEIVE BIT
SEND BIT
Rx BIT INVALID
RESET DETECTED
END OF Tx BIT
COMPARE RECEIVED BIT
RESET DETECTED
454

Fig. 8

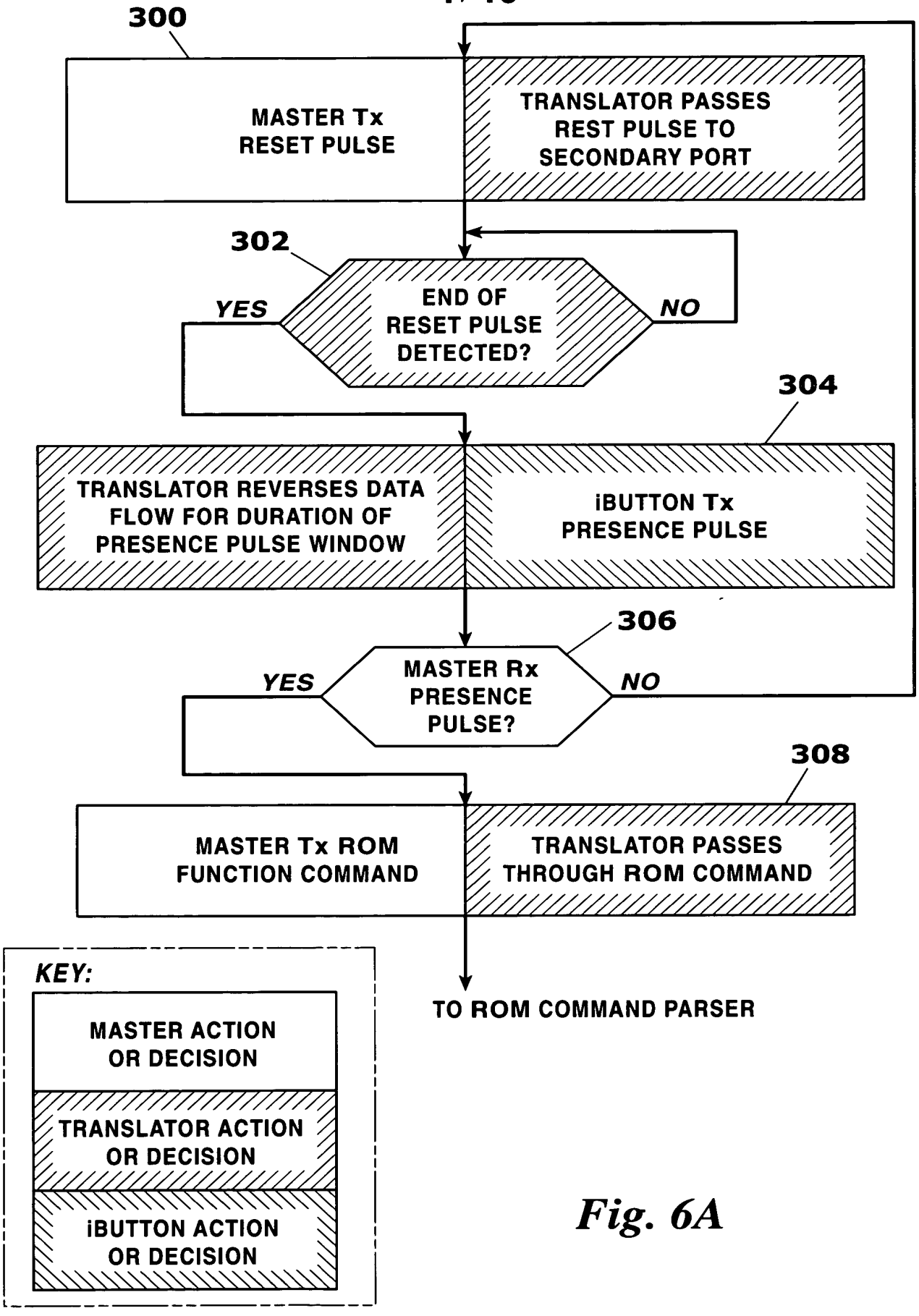

300
MASTER Tx RESET PULSE
TRANSLATOR PASSES REST PULSE TO SECONDARY PORT
302
YES
END OF RESET PULSE DETECTED?
NO
304
TRANSLATOR REVERSES DATA FLOW FOR DURATION OF PRESENCE PULSE WINDOW
iBUTTON Tx PRESENCE PULSE
306
YES
MASTER Rx PRESENCE PULSE?
NO
308
MASTER Tx ROM FUNCTION COMMAND
TRANSLATOR PASSES THROUGH ROM COMMAND
TO ROM COMMAND PARSER
KEY:
MASTER ACTION OR DECISION
TRANSLATOR ACTION OR DECISION
iBUTTON ACTION OR DECISION

Fig. 6A

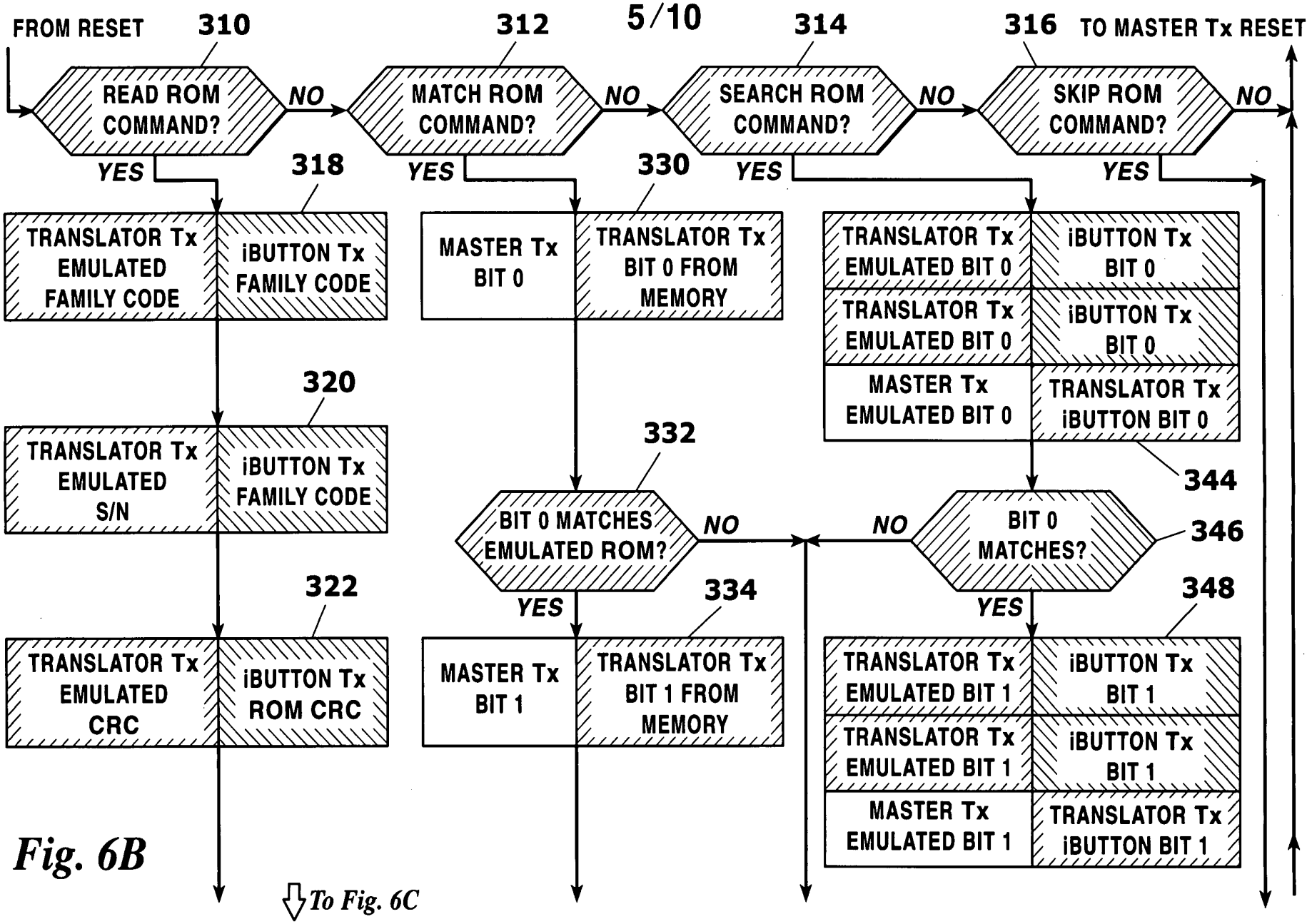


Fig. 6B

To Fig. 6C

Fig. 6C

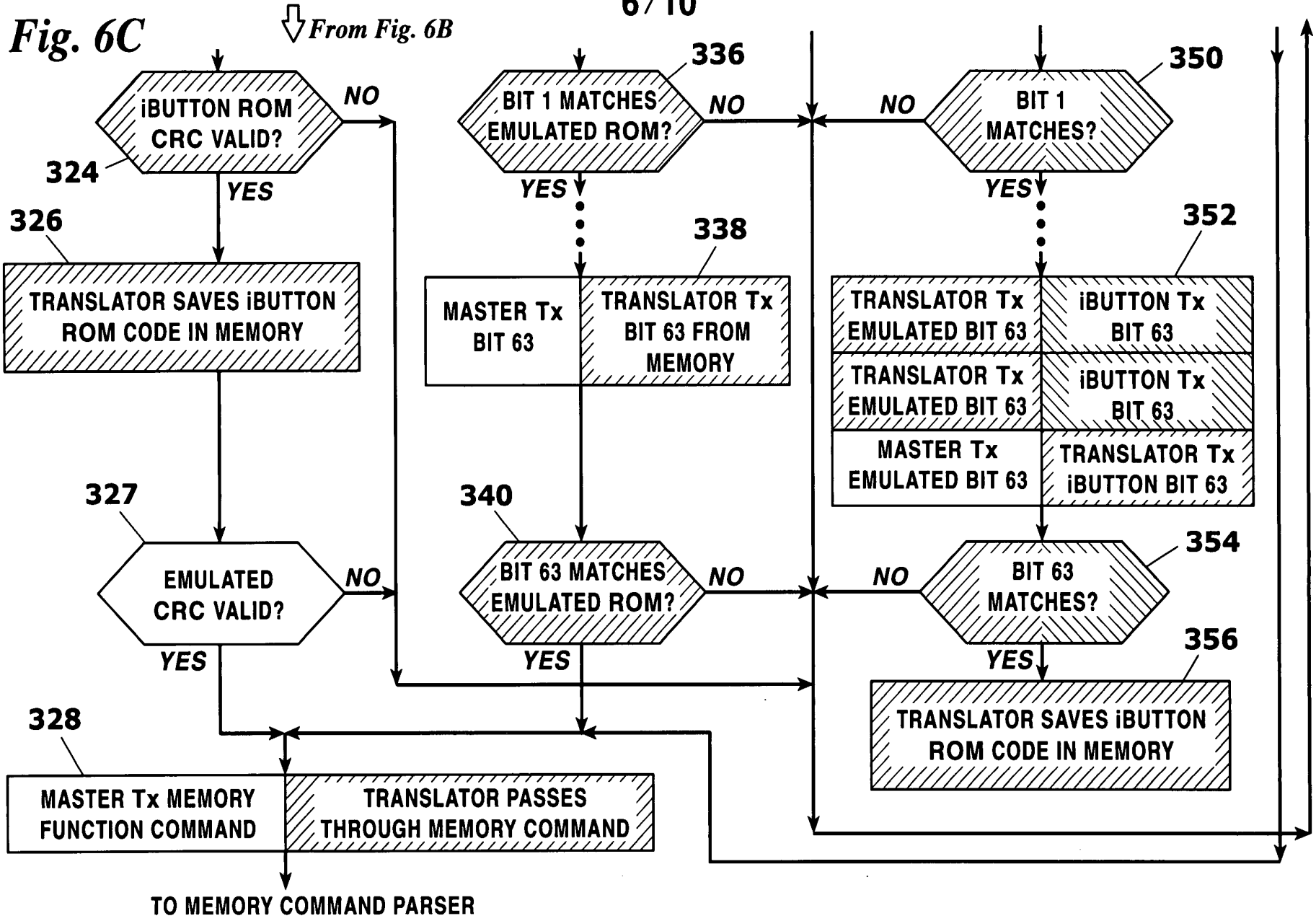
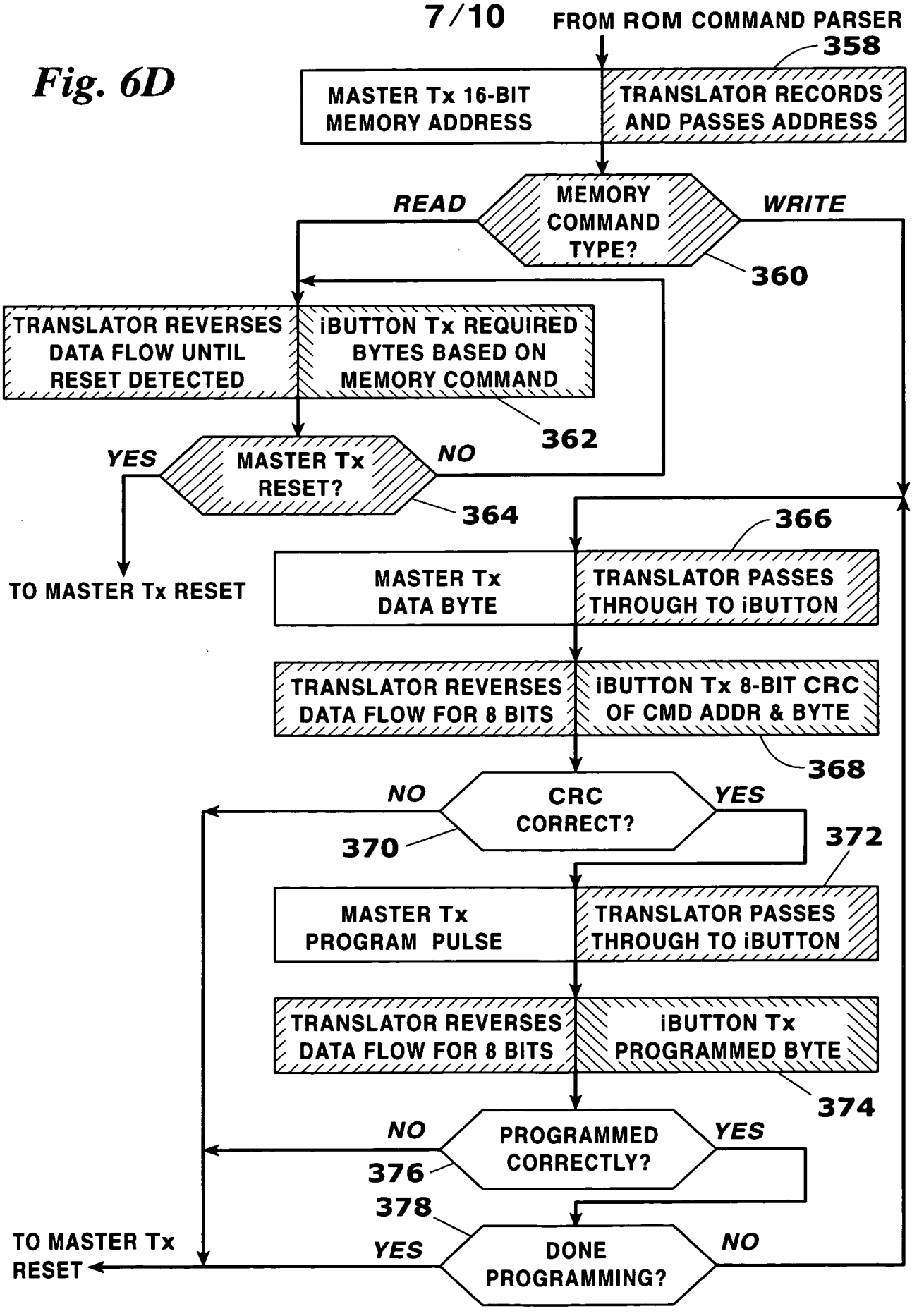


Fig. 6D


FROM ROM COMMAND PARSER
358
MASTER Tx 16-BIT MEMORY ADDRESS
TRANSLATOR RECORDS AND PASSES ADDRESS
READ
MEMORY COMMAND TYPE?
WRITE
360
TRANSLATOR REVERSES DATA FLOW UNTIL RESET DETECTED
iBUTTON Tx REQUIRED BYTES BASED ON MEMORY COMMAND
362
YES
MASTER Tx RESET?
NO
364
TO MASTER Tx RESET
366
MASTER Tx DATA BYTE
TRANSLATOR PASSES THROUGH TO iBUTTON
TRANSLATOR REVERSES DATA FLOW FOR 8 BITS
iBUTTON Tx 8-BIT CRC OF CMD ADDR & BYTE
368
NO
CRC CORRECT?
YES
370
372
MASTER Tx PROGRAM PULSE
TRANSLATOR PASSES THROUGH TO iBUTTON
TRANSLATOR REVERSES DATA FLOW FOR 8 BITS
iBUTTON Tx PROGRAMMED BYTE
374
NO
PROGRAMMED CORRECTLY?
YES
376
378
TO MASTER Tx RESET
YES
DONE PROGRAMMING?
NO

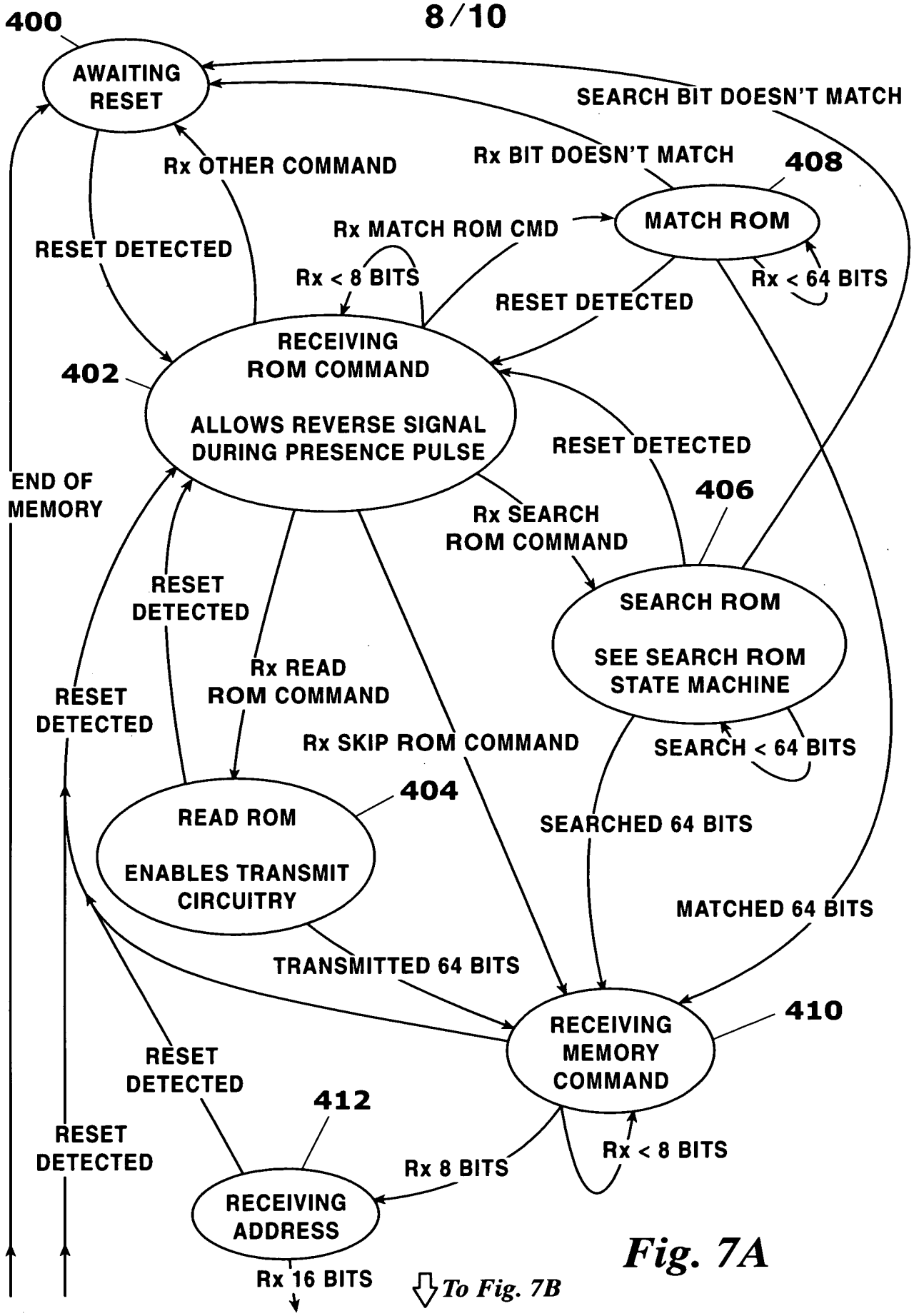
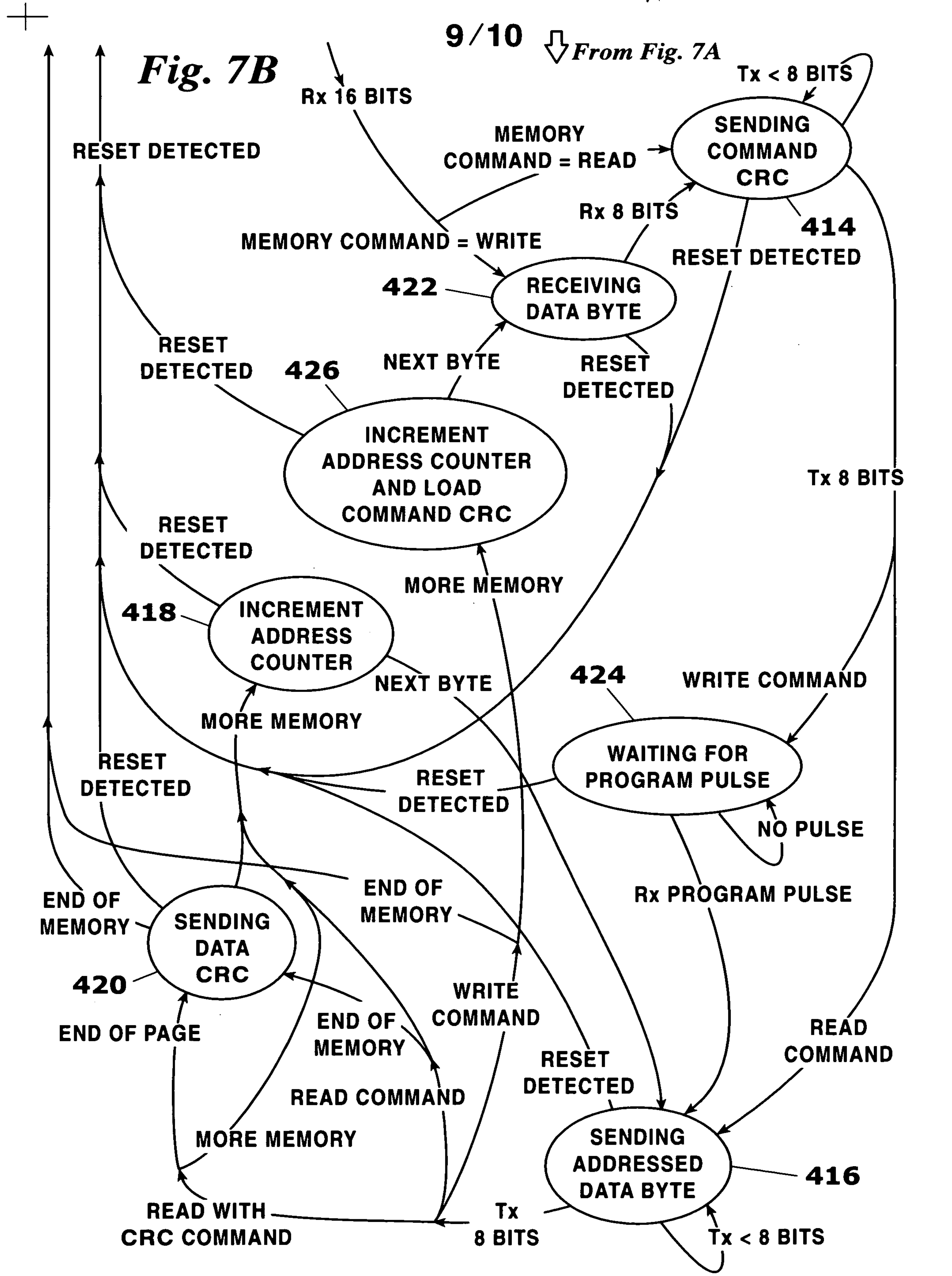

400
AWAITING RESET
SEARCH BIT DOESN'T MATCH
Rx OTHER COMMAND
Rx BIT DOESN'T MATCH
408
MATCH ROM
Rx MATCH ROM CMD
RESET DETECTED
Rx < 8 BITS
Rx < 64 BITS
RESET DETECTED
RECEIVING ROM COMMAND
402
ALLOWS REVERSE SIGNAL DURING PRESENCE PULSE
RESET DETECTED
406
END OF MEMORY
Rx SEARCH ROM COMMAND
RESET DETECTED
SEARCH ROM
SEE SEARCH ROM STATE MACHINE
Rx READ ROM COMMAND
RESET DETECTED
Rx SKIP ROM COMMAND
SEARCH < 64 BITS
404
READ ROM
ENABLES TRANSMIT CIRCUITRY
SEARCHED 64 BITS
MATCHED 64 BITS
TRANSMITTED 64 BITS
410
RECEIVING MEMORY COMMAND
RESET DETECTED
412
RESET DETECTED
Rx 8 BITS
Rx < 8 BITS
RECEIVING ADDRESS
Rx 16 BITS
To Fig. 7B

Fig. 7A

Fig. 7B


From Fig. 7A
Rx 16 BITS
RESET DETECTED
MEMORY COMMAND = READ
SENDING COMMAND CRC
Tx < 8 BITS
414
Rx 8 BITS
MEMORY COMMAND = WRITE
RESET DETECTED
422
RECEIVING DATA BYTE
RESET DETECTED
426
NEXT BYTE
RESET DETECTED
INCREMENT ADDRESS COUNTER AND LOAD COMMAND CRC
Tx 8 BITS
RESET DETECTED
MORE MEMORY
418
INCREMENT ADDRESS COUNTER
NEXT BYTE
424
WRITE COMMAND
MORE MEMORY
WAITING FOR PROGRAM PULSE
RESET DETECTED
RESET DETECTED
NO PULSE
Rx PROGRAM PULSE
END OF MEMORY
END OF MEMORY
SENDING DATA CRC
420
WRITE COMMAND
END OF PAGE
END OF MEMORY
READ COMMAND
RESET DETECTED
READ COMMAND
MORE MEMORY
SENDING ADDRESSED DATA BYTE
416
READ WITH CRC COMMAND
Tx 8 BITS
Tx < 8 BITS

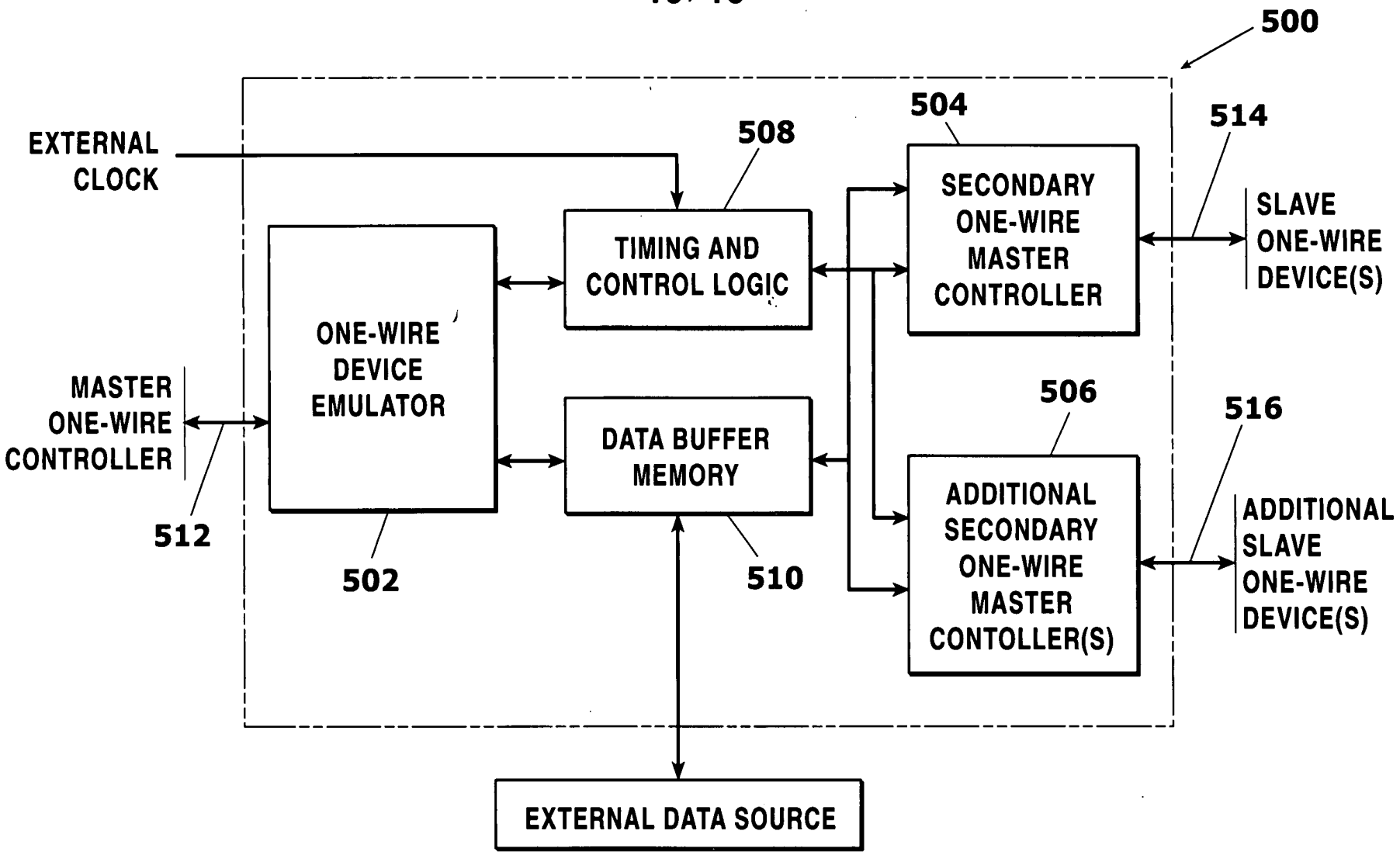

500
EXTERNAL CLOCK
508
504
514
SECONDARY ONE-WIRE MASTER CONTROLLER
SLAVE ONE-WIRE DEVICE(S)
TIMING AND CONTROL LOGIC
ONE-WIRE DEVICE EMULATOR
MASTER ONE-WIRE CONTROLLER
512
502
DATA BUFFER MEMORY
510
506
516
ADDITIONAL SECONDARY ONE-WIRE MASTER CONTOLLER(S)
ADDITIONAL SLAVE ONE-WIRE DEVICE(S)
EXTERNAL DATA SOURCE

Fig. 9